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| Tool Version : Vivado v.2018.3 (win64) Build 2405991 Thu Dec 6 23:38:27 MST 2018

| Date : Thu Oct 17 09:45:18 2024

| Host : Samuel running 64-bit major release (build 9200)

| Command : report\_utilization -file hello\_world\_arty\_a7\_utilization\_synth.rpt -pb hello\_world\_arty\_a7\_utilization\_synth.pb

| Design : hello\_world\_arty\_a7

| Device : 7a100ticsg324-1L

| Design State : Synthesized

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Utilization Design Information

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1. Slice Logic

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| Site Type | Used | Fixed | Available | Util% |

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| Slice LUTs\* | 2400 | 0 | 63400 | 3.79 |

| LUT as Logic | 2400 | 0 | 63400 | 3.79 |

| LUT as Memory | 0 | 0 | 19000 | 0.00 |

| Slice Registers | 1768 | 0 | 126800 | 1.39 |

| Register as Flip Flop | 1768 | 0 | 126800 | 1.39 |

| Register as Latch | 0 | 0 | 126800 | 0.00 |

| F7 Muxes | 339 | 0 | 31700 | 1.07 |

| F8 Muxes | 0 | 0 | 15850 | 0.00 |

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\* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt\_design after synthesis, if not already completed, for a more realistic count.

1.1 Summary of Registers by Type

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| Total | Clock Enable | Synchronous | Asynchronous |

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| 0 | \_ | - | - |

| 0 | \_ | - | Set |

| 0 | \_ | - | Reset |

| 0 | \_ | Set | - |

| 0 | \_ | Reset | - |

| 0 | Yes | - | - |

| 0 | Yes | - | Set |

| 0 | Yes | - | Reset |

| 88 | Yes | Set | - |

| 1680 | Yes | Reset | - |

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2. Memory

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| Site Type | Used | Fixed | Available | Util% |

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| Block RAM Tile | 2 | 0 | 135 | 1.48 |

| RAMB36/FIFO\* | 2 | 0 | 135 | 1.48 |

| RAMB36E1 only | 2 | | | |

| RAMB18 | 0 | 0 | 270 | 0.00 |

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\* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

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| Site Type | Used | Fixed | Available | Util% |

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| DSPs | 0 | 0 | 240 | 0.00 |

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4. IO and GT Specific

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| Site Type | Used | Fixed | Available | Util% |

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| Bonded IOB | 3 | 0 | 210 | 1.43 |

| Bonded IPADs | 0 | 0 | 2 | 0.00 |

| PHY\_CONTROL | 0 | 0 | 6 | 0.00 |

| PHASER\_REF | 0 | 0 | 6 | 0.00 |

| OUT\_FIFO | 0 | 0 | 24 | 0.00 |

| IN\_FIFO | 0 | 0 | 24 | 0.00 |

| IDELAYCTRL | 0 | 0 | 6 | 0.00 |

| IBUFDS | 0 | 0 | 202 | 0.00 |

| PHASER\_OUT/PHASER\_OUT\_PHY | 0 | 0 | 24 | 0.00 |

| PHASER\_IN/PHASER\_IN\_PHY | 0 | 0 | 24 | 0.00 |

| IDELAYE2/IDELAYE2\_FINEDELAY | 0 | 0 | 300 | 0.00 |

| ILOGIC | 0 | 0 | 210 | 0.00 |

| OLOGIC | 0 | 0 | 210 | 0.00 |

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5. Clocking

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| Site Type | Used | Fixed | Available | Util% |

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| BUFGCTRL | 2 | 0 | 32 | 6.25 |

| BUFIO | 0 | 0 | 24 | 0.00 |

| MMCME2\_ADV | 0 | 0 | 6 | 0.00 |

| PLLE2\_ADV | 0 | 0 | 6 | 0.00 |

| BUFMRCE | 0 | 0 | 12 | 0.00 |

| BUFHCE | 0 | 0 | 96 | 0.00 |

| BUFR | 0 | 0 | 24 | 0.00 |

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6. Specific Feature

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| Site Type | Used | Fixed | Available | Util% |

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| BSCANE2 | 0 | 0 | 4 | 0.00 |

| CAPTUREE2 | 0 | 0 | 1 | 0.00 |

| DNA\_PORT | 0 | 0 | 1 | 0.00 |

| EFUSE\_USR | 0 | 0 | 1 | 0.00 |

| FRAME\_ECCE2 | 0 | 0 | 1 | 0.00 |

| ICAPE2 | 0 | 0 | 2 | 0.00 |

| PCIE\_2\_1 | 0 | 0 | 1 | 0.00 |

| STARTUPE2 | 0 | 0 | 1 | 0.00 |

| XADC | 0 | 0 | 1 | 0.00 |

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7. Primitives

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| Ref Name | Used | Functional Category |

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| FDRE | 1680 | Flop & Latch |

| LUT6 | 1270 | LUT |

| LUT5 | 584 | LUT |

| LUT4 | 416 | LUT |

| MUXF7 | 339 | MuxFx |

| LUT3 | 263 | LUT |

| CARRY4 | 158 | CarryLogic |

| LUT2 | 94 | LUT |

| FDSE | 88 | Flop & Latch |

| LUT1 | 11 | LUT |

| RAMB36E1 | 2 | Block Memory |

| IBUF | 2 | IO |

| BUFG | 2 | Clock |

| OBUF | 1 | IO |

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8. Black Boxes

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| Ref Name | Used |

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9. Instantiated Netlists

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| Ref Name | Used |

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